depth direction, the averaged concentration of phosphorus increases from the channel formation region 121A toward the third impurity region 126A.

IN THE CLAIMS:

Please amend claims 13, 14 and 16 as follows:

13. (Amended) A semiconductor device comprising:

a semiconductor island on an insulating surface;

source and drain regions formed in the semiconductor island;

a channel region in the semiconductor island between the source and drain regions;

a pair of LDD regions formed between the channel region and the source and drain regions;

a gate electrode formed over the semiconductor island with a gate insulating film interposed therebetween wherein said gate electrode comprises at least a first conductive layer and a second conductive layer formed on the first conductive layer, said first conductive layer having a pair of tapered portions, which extend beyond side edges of the second conductive layer,

wherein the pair of the LDD regions has a pair of first portions which are overlapped by the pair of the tapered portions of the first conductive layer, and a pair of second portions which extend beyond side edges of the first conductive layer.

14. (Amended) A device according to claim 13, wherein an angle between the tapered portions of the first conductive layer and the gate insulating film is in a range of 3 to 60 degrees.

16. (Amended) A device according to claim 13, wherein the first conductive layer includes at least one selected from the group consisting of chromium (Cr), tantalum (Ta) an n-type silicon containing phosphorus, titanium (Ti), tungsten (W), and molybdenum (Mo) while the second conductive layer includes at least one selected from the group consisting of aluminum (Al), copper (Cu), chromium (Cr), tantalum (Ta),

titanium (Ti), tungsten (W), molybdenum (Mo), an n-type silicon containing phosphorus, and silicide.